IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. Claims 1, 20, and 24 have been amended.

1. (Currently Amended) A die, comprising:

a dielectric layer positioned on top of a semiconductor support layer;

a via passing through the dielectric layer and the semiconductor support layer, wherein a first end of the via is positioned in the dielectric layer and a second end of the via is positioned in the semiconductor support layer, wherein a first diameter of the first end is greater than a second diameter of the second end, wherein the second end of the via includes a shaft in the semiconductor support layer, the shaft including a shaft diameter similar to the second diameter, wherein the shaft tapers outward from a center of the via within the semiconductor support layer towards the dielectric layer to form a semi-cone shape in the semiconductor support layer, wherein the semi-cone shape forms an increased via contact area at the first end for coupling the via to a [[the]] contact; and

the [[a]] contact positioned on top of the dielectric layer, the contact coupled to the first end of the via.

2. (Canceled)

3. (Canceled)

4. (Previously Presented) The die of claim 1 wherein the via continues to taper outwards from the second end into the first end to form a semi-cone shape in the dielectric layer.

5. (Previously Presented) The die of claim 1 wherein a diameter of the first end is similar to a diameter of the semi-cone shape, the first end to form a cylinder shape in the dielectric layer.

6. (Canceled)

7. (Previously Presented) The die of claim 1 wherein the via includes a metal-filled via.

Claims 8-19 (Canceled).

20. (Currently Amended) A die package, comprising:

a semiconductor support layer;

a dielectric layer disposed on the semiconductor support layer;

a via including a first end and a second end, the first end positioned in the dielectric layer and the second end positioned in the semiconductor support layer, wherein a diameter of the first end is greater than a diameter of the second end, wherein the second end includes a shaft and an enlarged end in the semiconductor support layer, the enlarged end between the shaft and the first end, wherein the enlarged end tapers outward from a center of the via within the semiconductor support layer towards the dielectric layer, the enlarged end defining a semi-cone shape, wherein the enlarged end creates an increased via contact area at the first end for coupling the via to a [[the]] first contact;

the [[a]] first contact, disposed on the dielectric layer, coupled to the first end of the via; and

a second contact, disposed on the semiconductor support layer, coupled to the second end of the via, wherein the second contact to be mounted to a printed circuit board.

21. (Canceled)

22. (Previously Presented) The die package of claim 20 wherein the first end continues to taper outwards from the enlarged end to form a semi-cone shape in the dielectric layer.

23. (Previously Presented) The die package of claim 20 wherein a diameter of the first end of the via through the dielectric layer is similar to a diameter of the semi-cone shape, the first end to form a cylinder shape in the dielectric layer.

24. (Currently Amended) A system, comprising:

a printed circuit board (PCB); and

a processor coupled to the PCB, wherein the processor includes:

a dielectric layer positioned on top of a semiconductor support layer;

a via passing thro ugh the dielectric layer and the semiconductor support layer, wherein a first end of the via is positioned in the dielectric layer and a second end of the via is positioned in the semiconductor support layer, wherein a first diameter of the first end is greater than a second diameter of the second end, wherein the second end includes a shaft in the semiconductor support layer, the shaft including a shaft diameter similar to the second diameter, wherein the second end tapers outward from a center of the via within the semiconductor support layer towards the dielectric layer, the second end defining a semi-cone shape in the semiconductor support layer; and

a first contact positioned on top of the dielectric layer, the first contact coupled to the first end of the via, wherein the second end of the via is coupled to the PCB via a second contact.

25. (Canceled)

26. (Canceled)

27. (Original) The system of claim 24 wherein the first diameter is approximately twice the second diameter.